Ferroelectric memory transistor with resistively couple floating gate

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Inventor: BLACK CHARLES T (US); WELSER JEFFREY J (US)

Applicant: IBM (US)

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The present invention proposes a new type of single-transistor memory device, which stores information using the polarization of a ferroelectric material. The device is a floating-gate FET, with a ferroelectric material positioned between the gate and the floating gate, and a resistance, preferably in the form of a thin SiO2 dielectric between the floating gate and the transistor channel. Unlike previous designs, in this device the floating gate is both capacitively and

resistively coupled to the transistor channel, which enables the device to be both read and written using low voltages. This device offers significant advantages for operation at low voltages and at high speeds, for repeated cycling of over 1010 times, since device durability is limited by the ferroelectric endurance rather than oxide breakdown, and for integration at gigabit densities.